

Model Name : BIWB6/B7/E8
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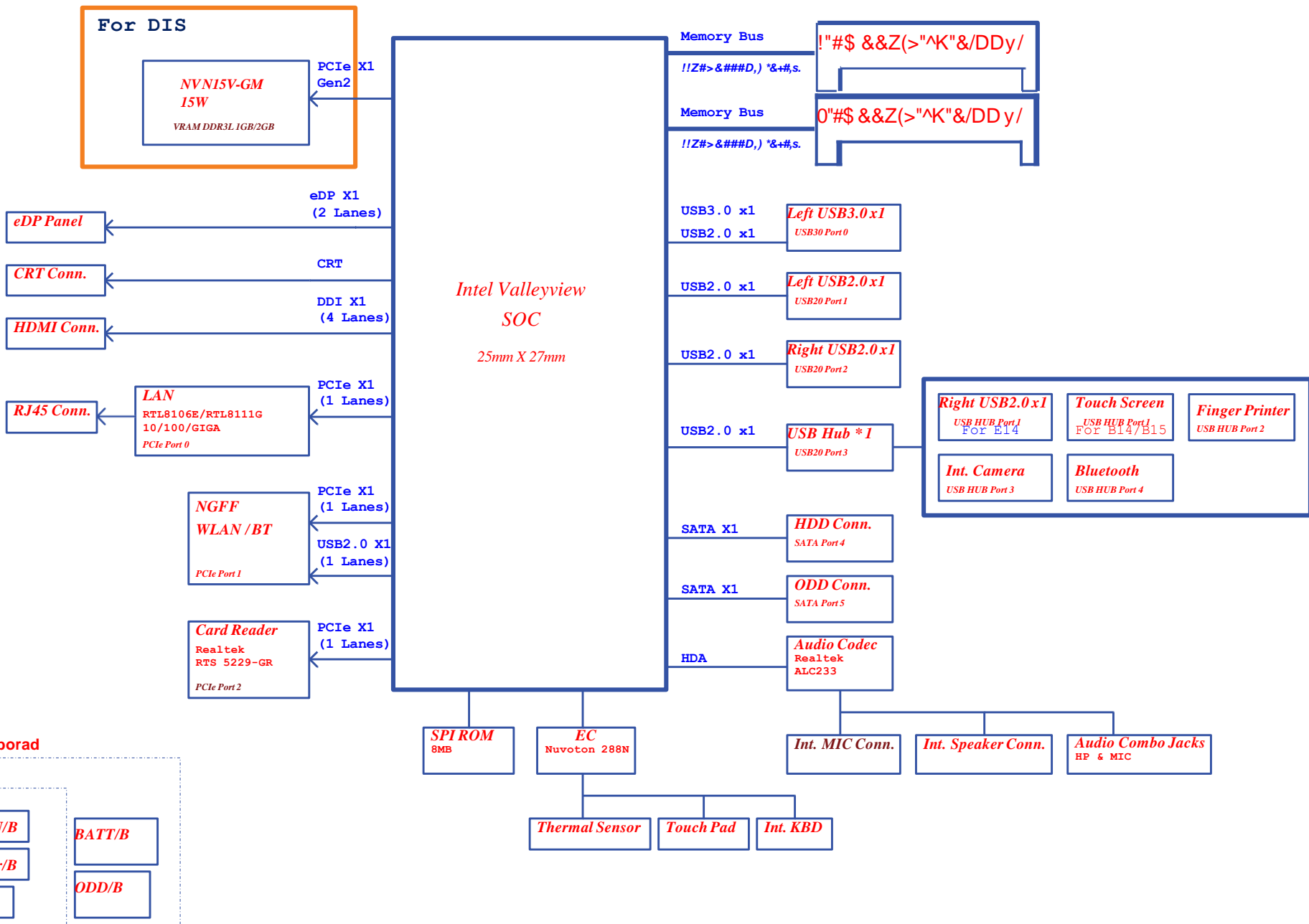
Compal Confidential

BIWB6/B7/E8 DIS M/B Schematics Document

Intel Bay Trail M

2014-02-10
REV:1.0

Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2013/04/12		Deciphered Date		2014/04/12		Title					
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
h2343	5
74229#>48	D65
y&W @89ABW4BC	y&W5
6D7 89;<89=92>	6D75
6D7 89;<89=92>;2343	56D75
6^& 89;<89=92>	6^&5
6^& 89;<89=92>;2343	56^&5
d4;# \$ ^#8992	d^5
0F6 GB4CGH;	0/E5
0F6 GB4CGH;	0/D5
0F6 GB4CGH;	6/E5

EC SM Bus1 address

Device	Address
Smart Battery	0001_011Xb
Charger	0b00010010(0x12H)

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

EC SM Bus2 address

Device	Address
GPU	0x9E
Thermal	1001_101xb

43 level BOM table

43 Level	Description	BOM Structure

USOC1
N2920@

S IC FH8065301616203 SR1SF B3 1.86G C38! S IC FH8065301616103 SR1SE B3 2.17G C38!
Part Number = SA00007E860 Part Number = SA00007E990

USOC1
N3520@

USOC1
N2815@

S IC FH8065301619509 SR1SJ B3 1.86G C38!
Part Number = SA00007EO50

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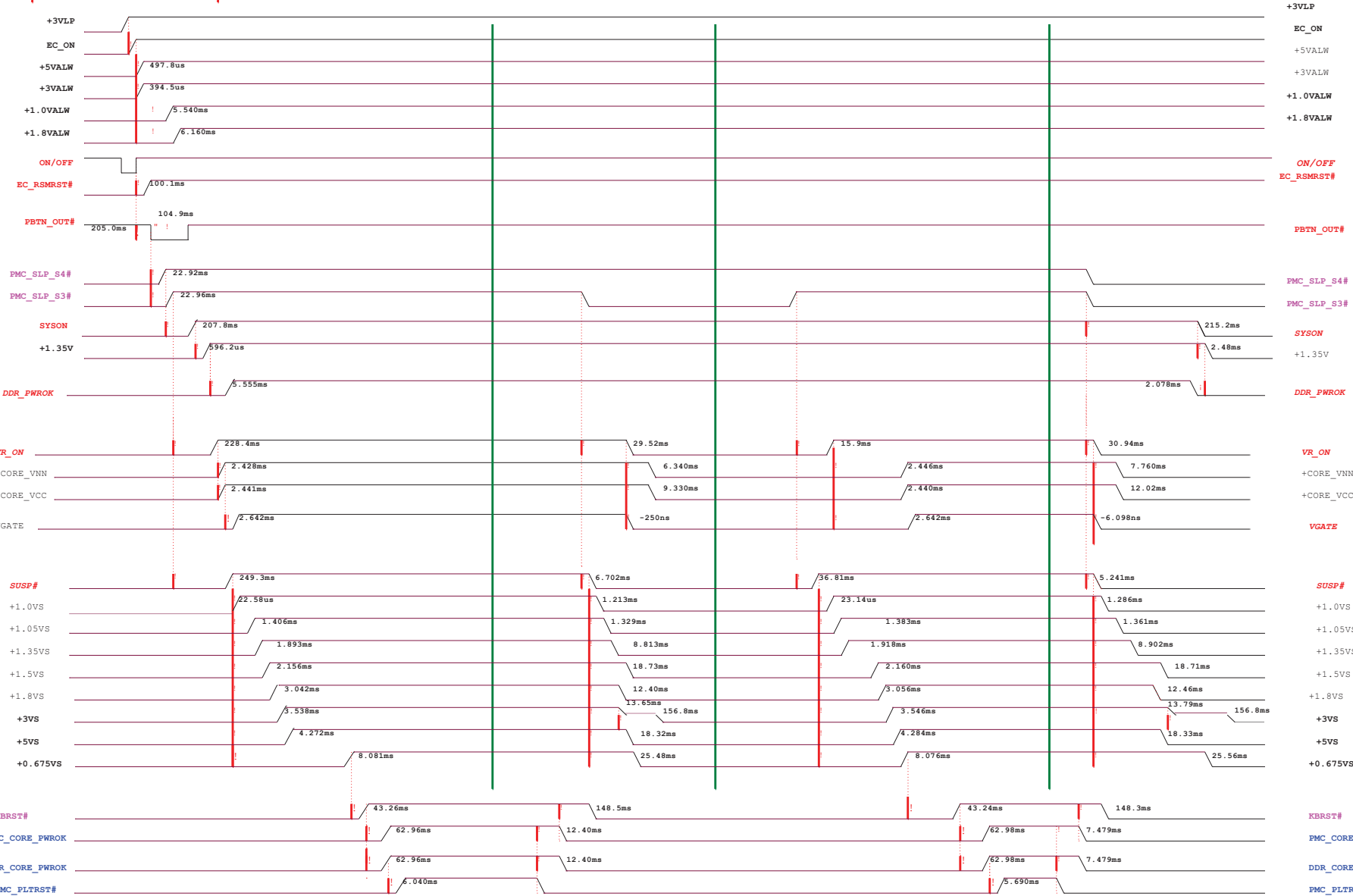
Power On

S3

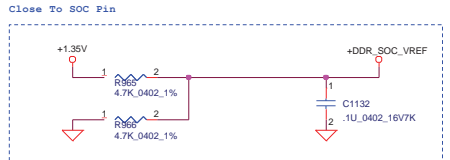
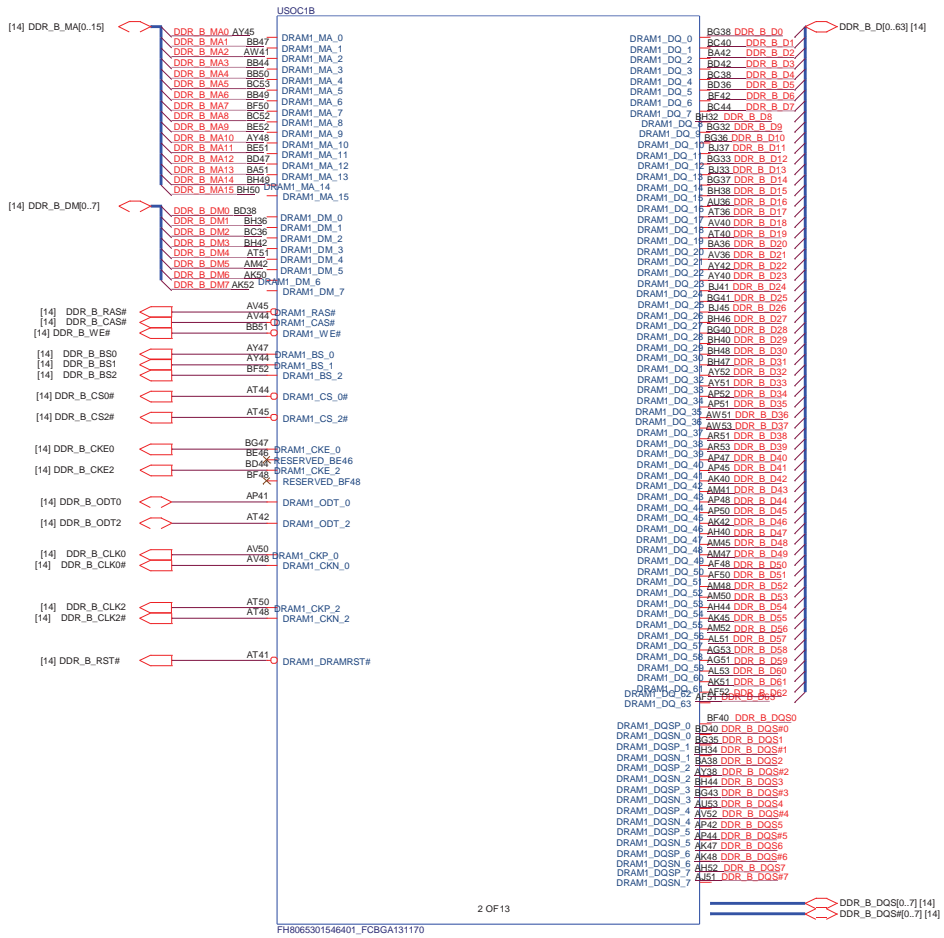
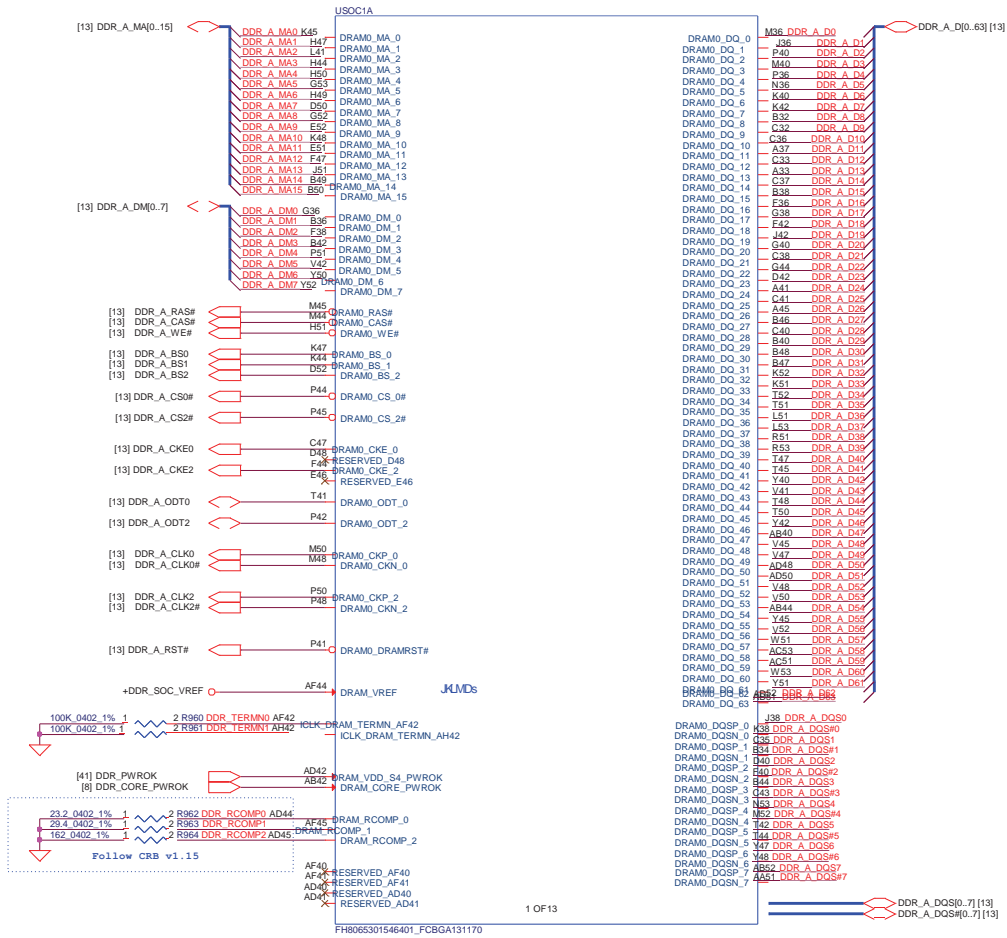
S3 Resume

Power Off

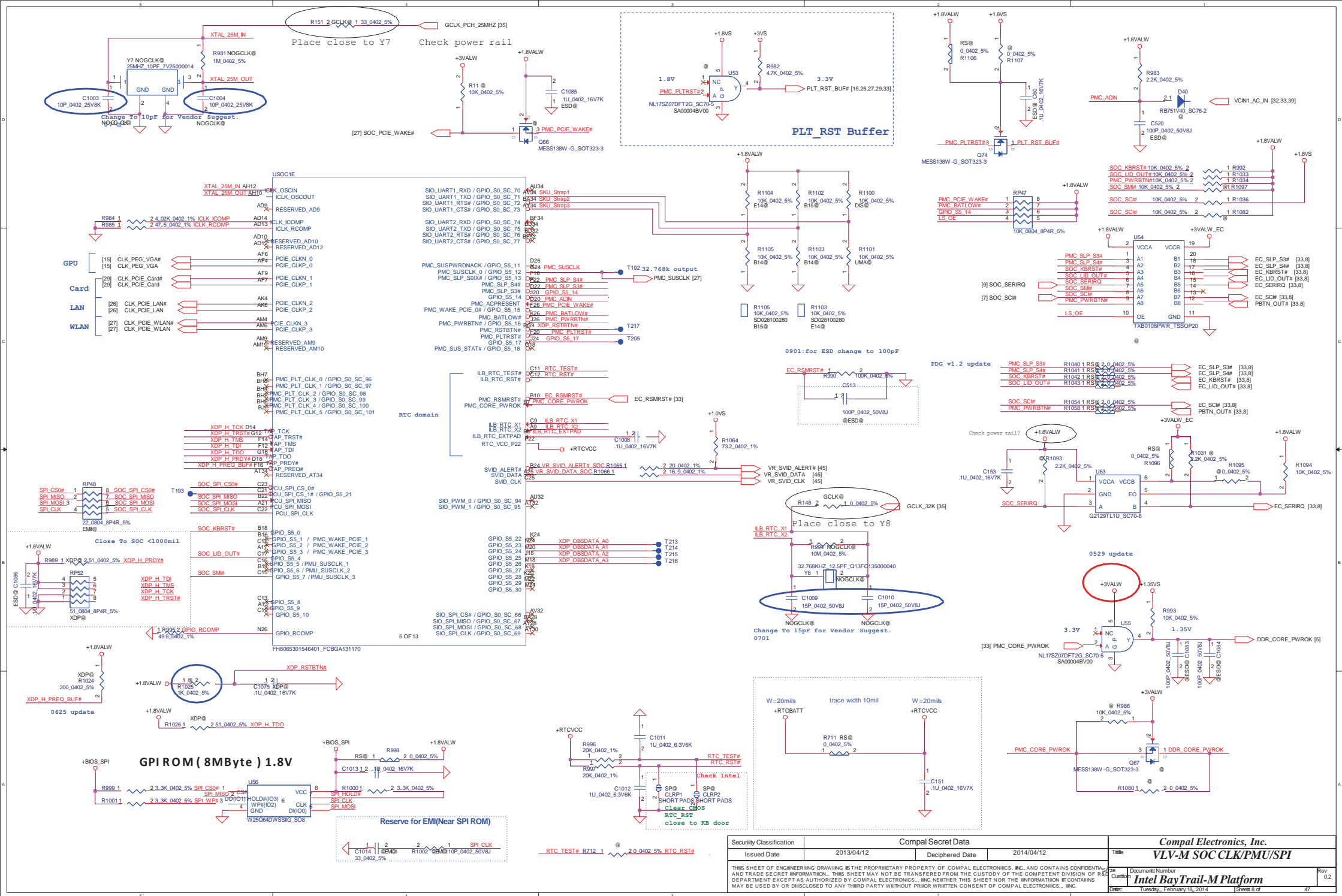
Plug in



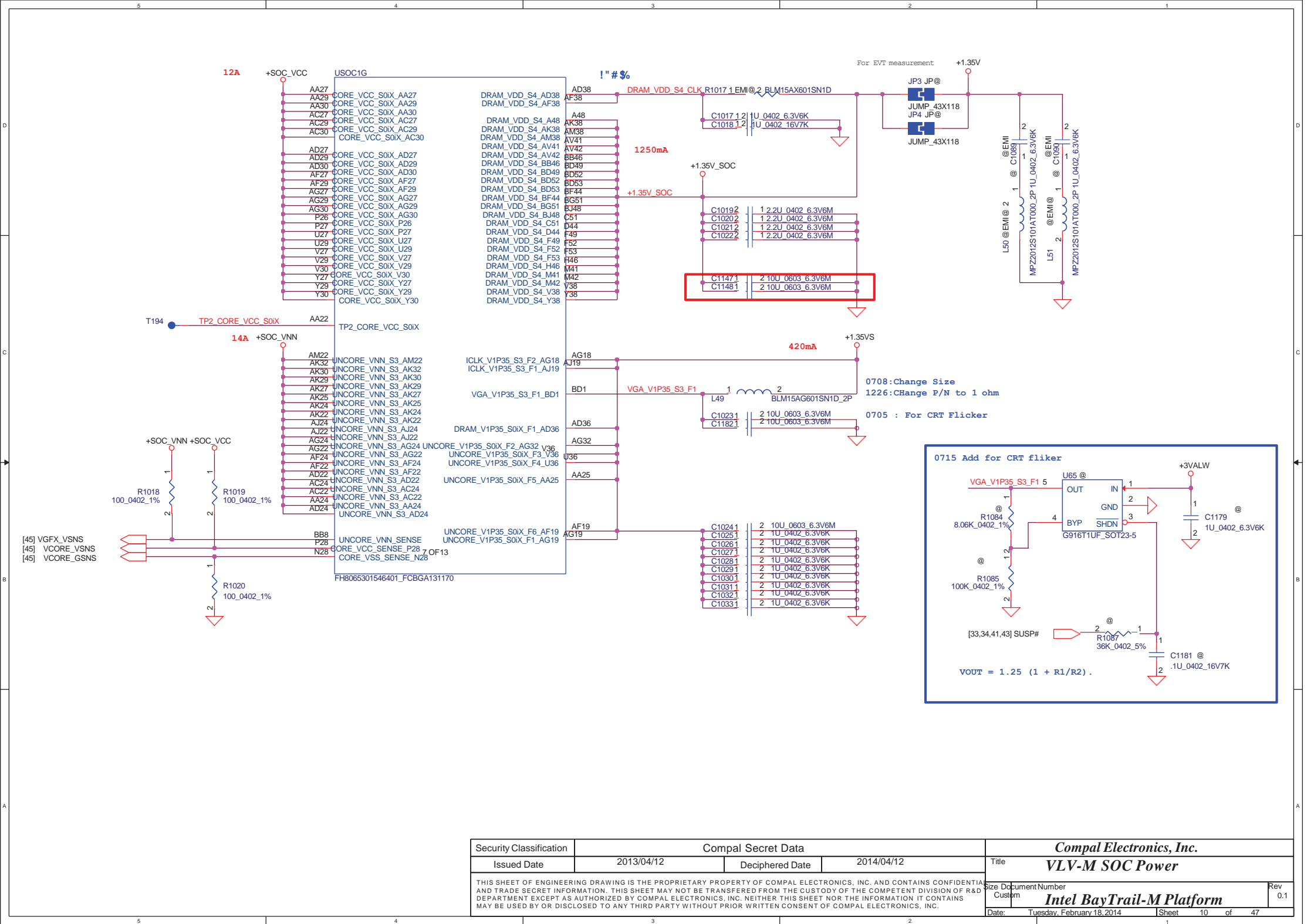
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2013/04/12		2014/04/12		Power Sequence		
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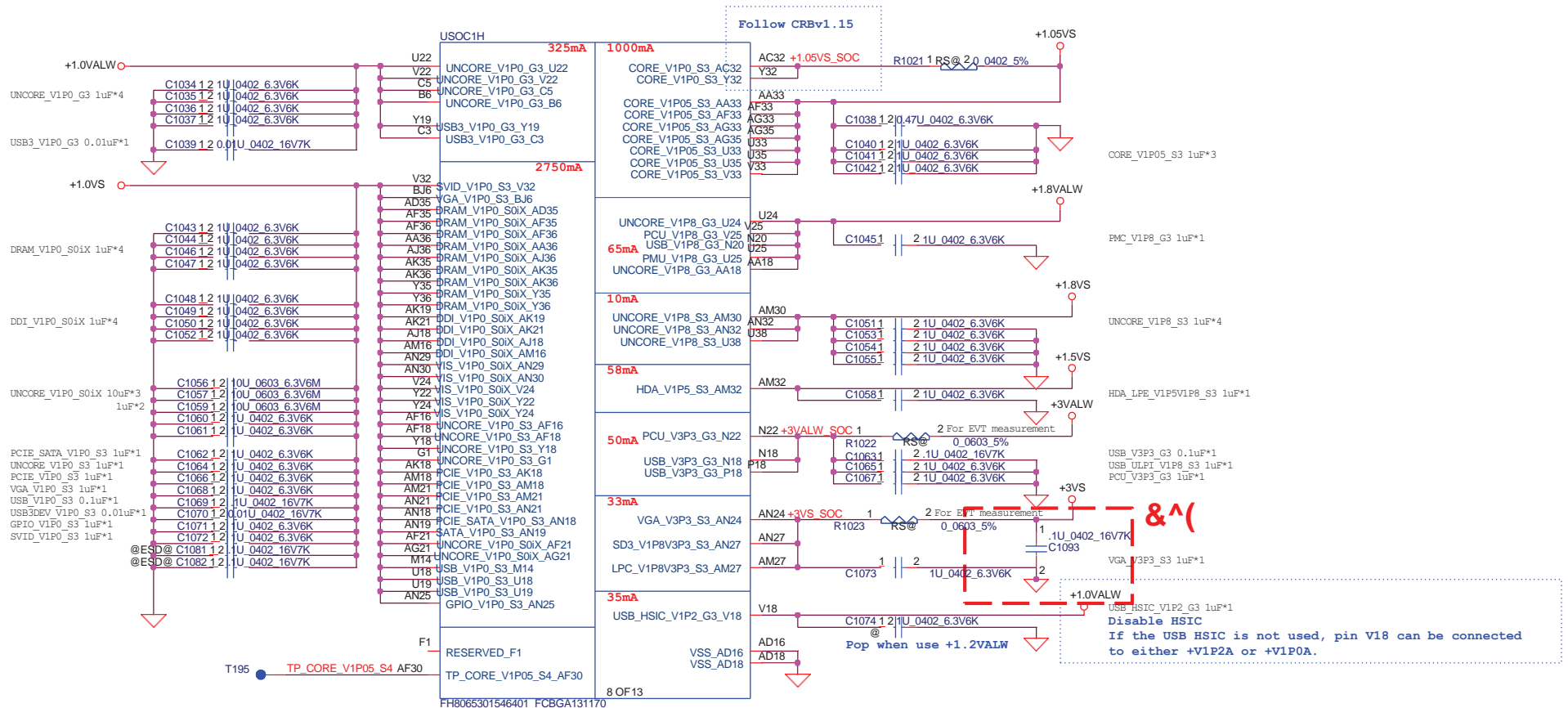


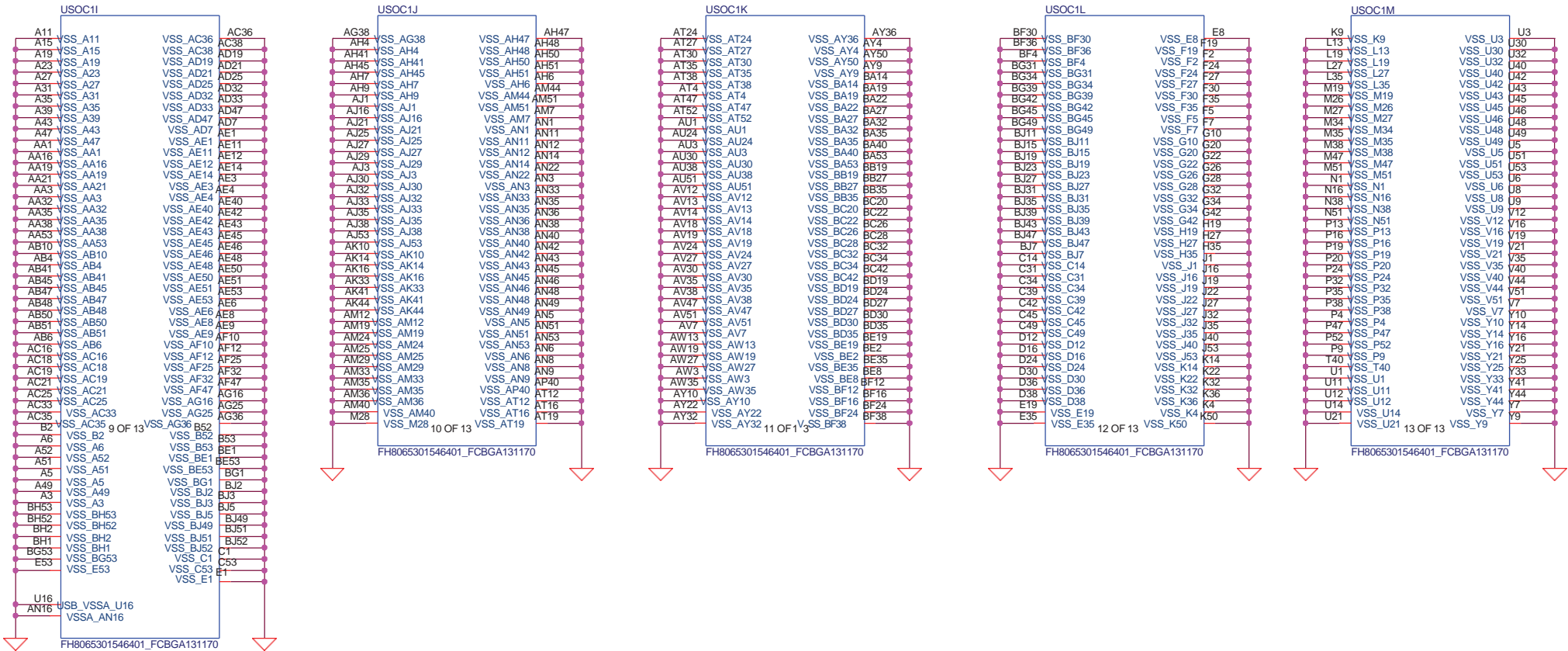
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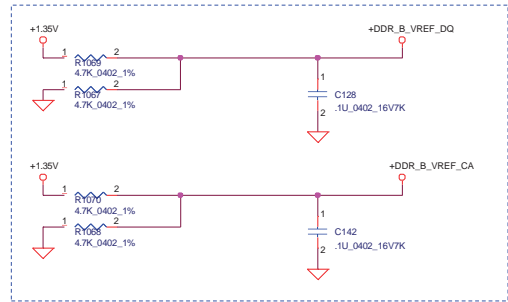
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2013/04/12	Deciphered Date	2014/04/12	VLV-M SOC CLK/PMU/SPI	
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All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM2.203,204

Channel B

<Address: SA0:SA1=10 (A2H)>
DIMM_2 REV H:4mm

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PCIE CLK
(From SOC)

PCIE X1 Bus
(Link to SOC)

[8] CLK_PEG_VGA
CLK_PEG_VGA#
[7] POE_PRX_DTX_P0
[7] POE_PRX_DTX_N0

POE_PRX_DTX_P0 CV11 DS@ 1.2 1U 0402 16V7K POE_GTX_HRX_PS0 AC9
POE_PRX_DTX_N0 CV12 DS@ 1.2 1U 0402 16V7K POE_GTX_HRX_PS0 AC9

POE_PTX_C_DRX_P0
POE_PTX_C_DRX_N0

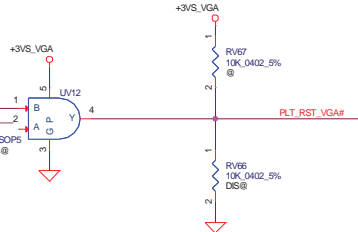
Reset Control

(From SOC GPIO)
(From SOC GPIO)

[26,27,29,33,8] PLT_RST_BUF#
[9] DGPU_HOLD_RST#

PLT_RST_BUF#
DGPU_HOLD_RST#

TC7SH08FUF SSOP5
DS@



Level shift & Isolation

[20,44] DGPU_PWRK

(From VGA_CORE VR)

[7] VGA_CLKREQ#

(To SOC)

1.8VS already pull high 10K at soc side

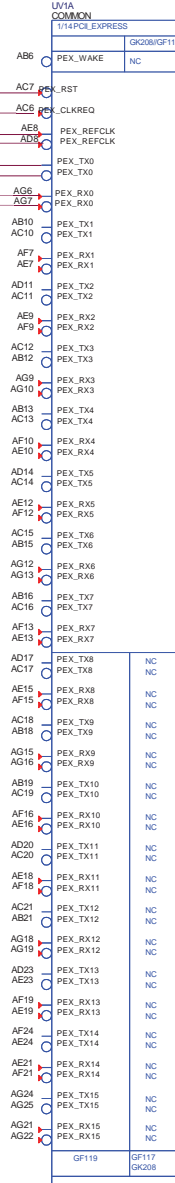
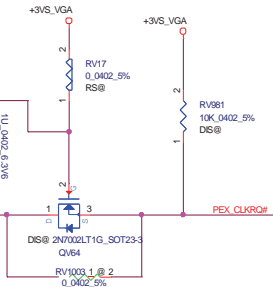
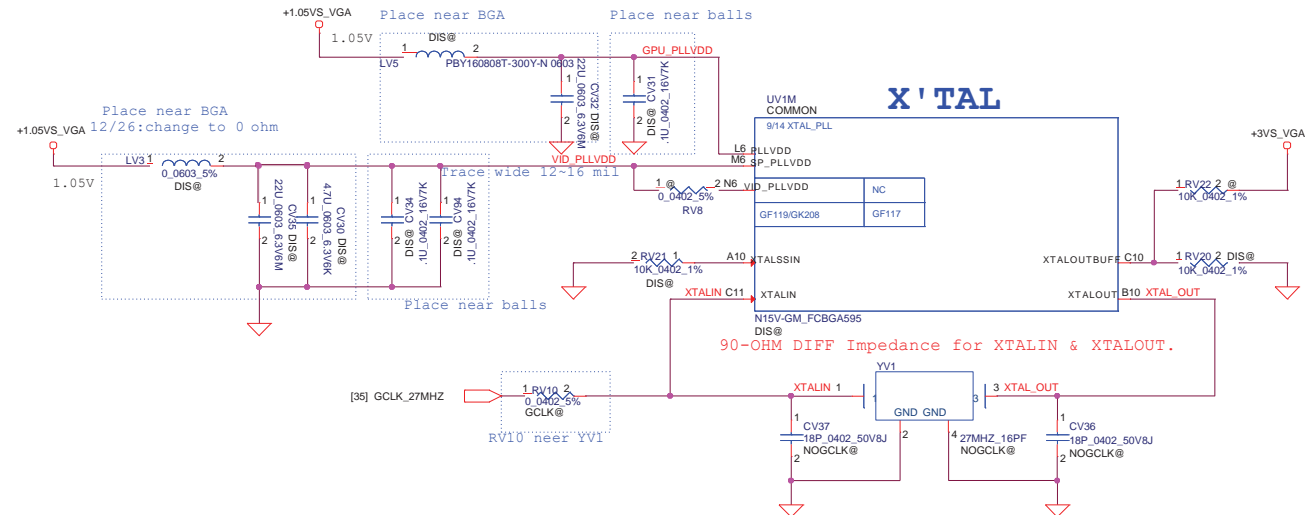
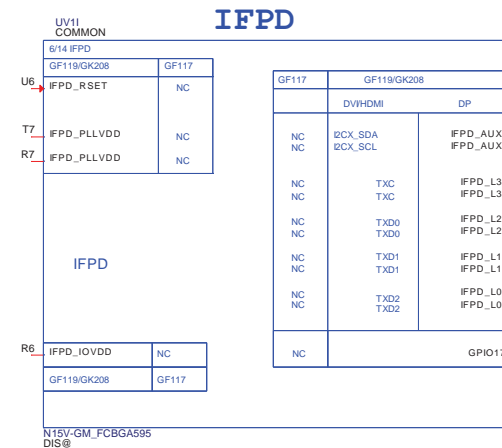
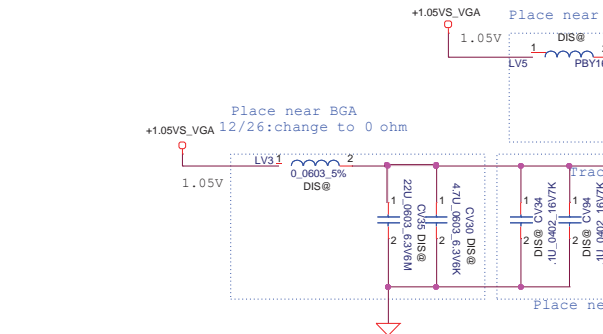
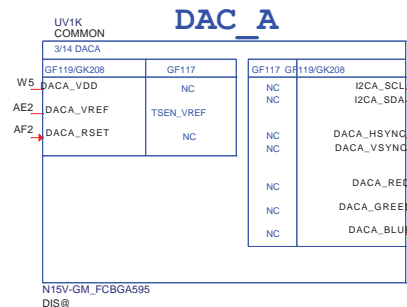


Table 3. PEX10VDD/Q Decoupling

Capacitor Type	Typical N14x Population	N15V-GM Population	N155-GV Population	N155-GM-GT Population	Location
10uF	X85	0402	4	4	Under GPU
10uF	X85	0402	2	2	Under GPU
10uF	X58	0805	4	4	Near GPU
22uF	X58	0805	4	4	Near GPU

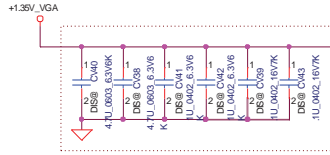
To POWER

trace width: 16mils
differential voltage sensing.
differential signal routing.

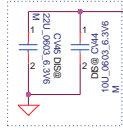


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Place under GPU



Place near GPU



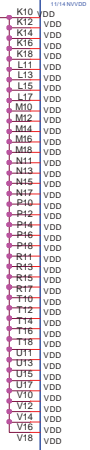
UV/D
COMMON



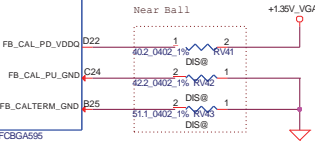
GPU_Decoupling CAPs @ Power Page

+VGA CORE
Voltage by GPU SKU

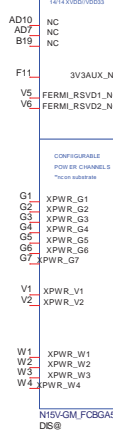
UV/E
COMMON



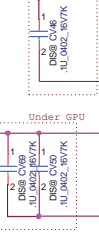
Near Ball



UV/C
COMMON



Under GPU

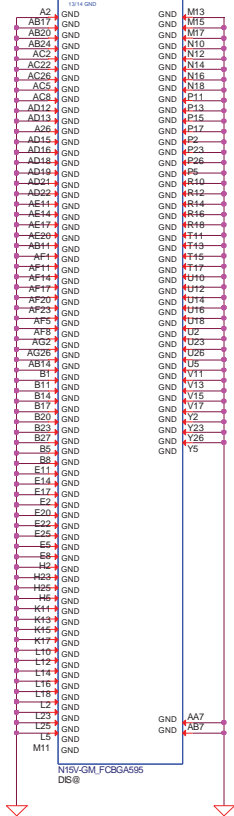


Near GPU



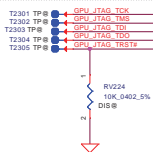
** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

UV/F
COMMON

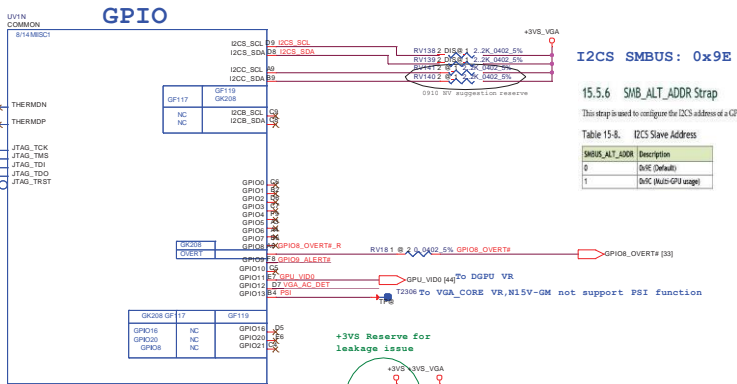


- VGA_THERMON and VGA_THERMOP:
1. 5mil track width and spacing
 2. 5mil grounded guard tracks width and spacing
 3. ground referenced
 4. Connect guard tracks to pin5

For BSC using.



GPIO



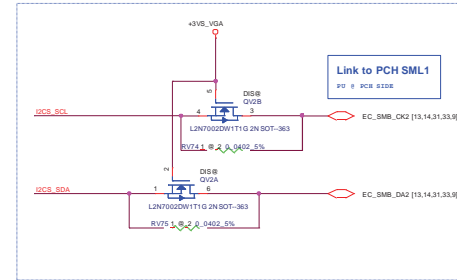
I2CS SMBUS: 0x9E

15.5.6 SMB_ALT_ADDR Strap
This strap is used to configure the I2CS address of a GPU or the I2CS slave address.

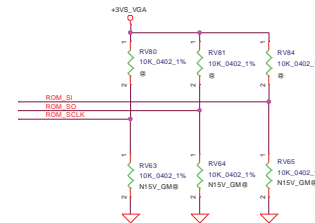
Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9F (Multi-GPU usage)

Internal Thermal Sensor



STRAP

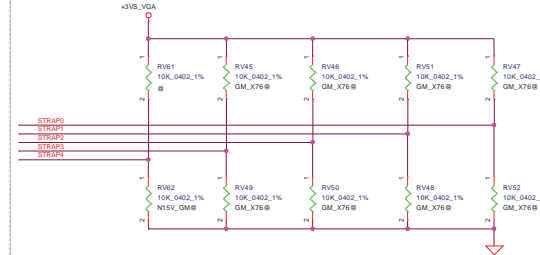


N15V-GM Binary Straps

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10K	Pull-down to GND
ROM_SI	SMB_VENOR	10K	-Pull-up to 3V3 (BIOS ROM ends) -Pull-down to GND if no BIOS ROM
ROM_SO	VGA_DEVICE	10K	Pull-down to GND (no display)

STRAP



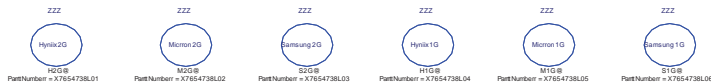
N15V-GM Binary Straps

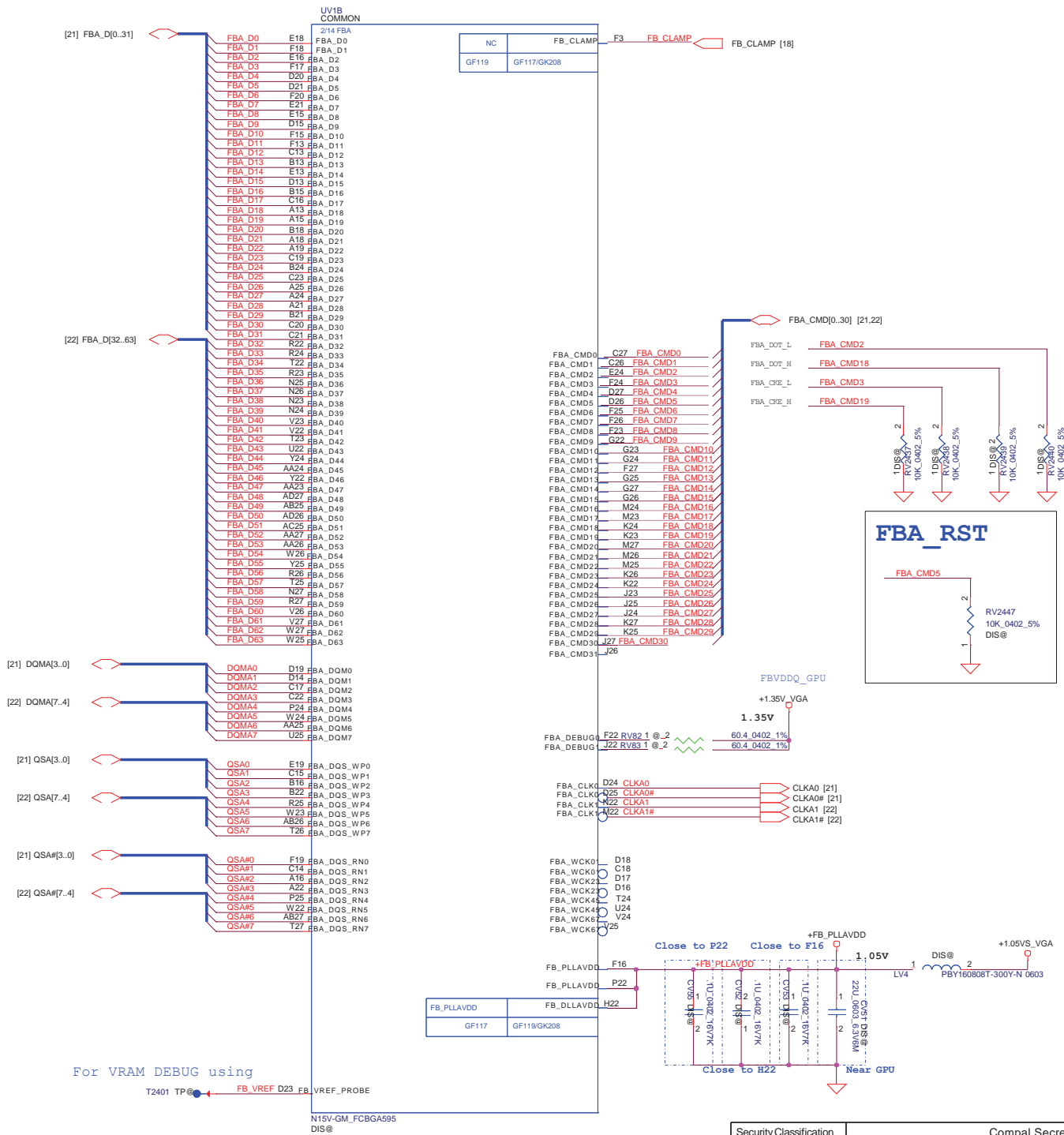
Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
STRAP0	RAM_CFG[0]	10K	See note below
STRAP1	RAM_CFG[1]	10K	See note below
STRAP2	RAM_CFG[2]	10K	See note below
STRAP3	RAM_CFG[3]	10K	See note below
STRAP4	PCIE_MAX_SPEED	10K	Pull-down to GND

N15V-GM VRAM Straps:

RAM_CFG (3..0)
[ROM_SI (3..0)]





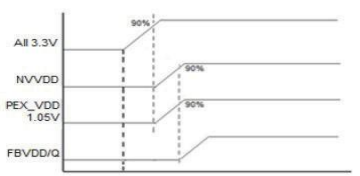
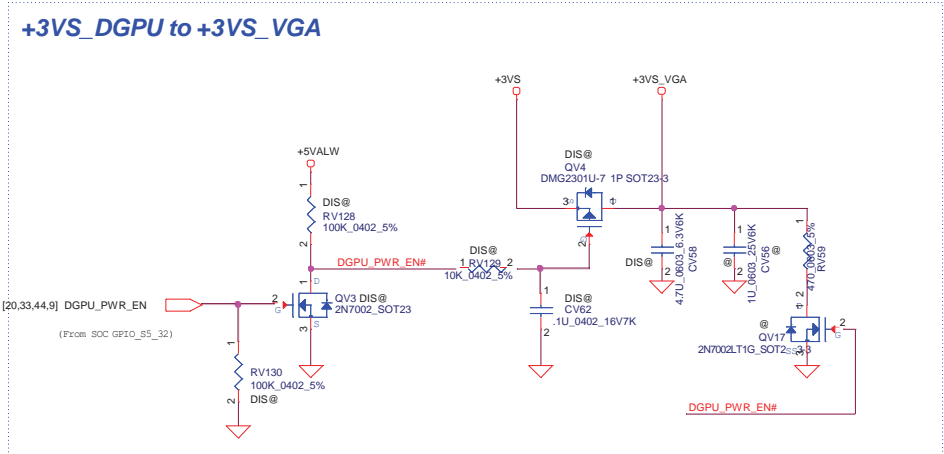
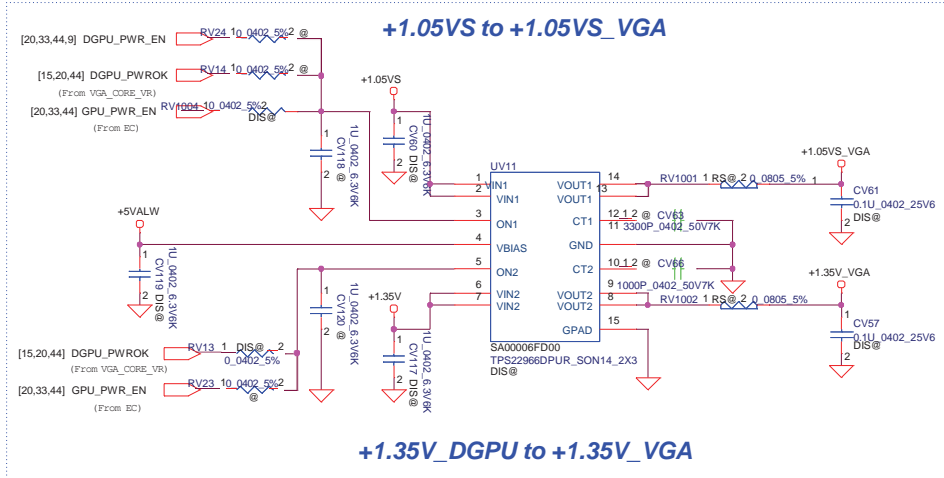
6.1.10 Memory ODTx, CKEx, and RST Termination

DDR3 requires Memory Termination on CKEx, ODTx and Memory Reset (RST). Table 6-8 describes the required termination.

Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 k
CKEx	10 k
RST	10 k
CS*	No Termination

For VRAM DEBUG using
T2401 TP@ FB_VREF D23 FB_VREF_PROBE



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

Note:
• The ramp time for any rail must be more than 10 μ s and is recommended to be less than 2ms.

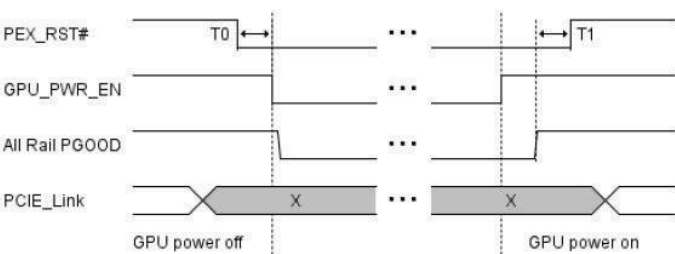
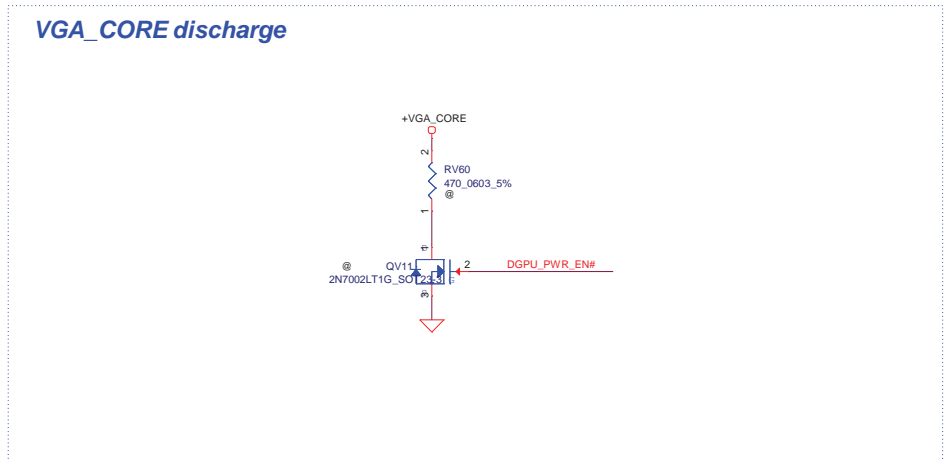


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Memory Partition A - Lower 32 bits [31..0]

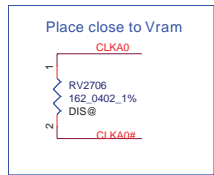
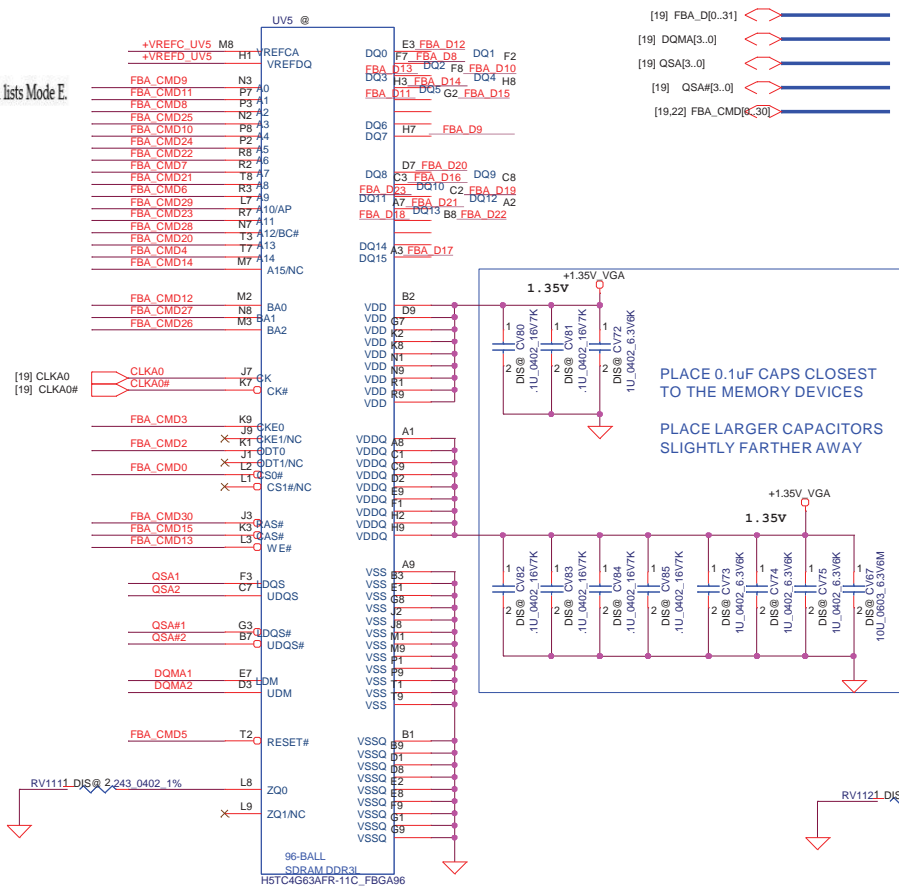
Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

Table 6-3. Mode D Command Mapping

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD16	CS0*	
FBx_CMD17		
FBx_CMD18	ODT	
FBx_CMD19	CKE	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33 ¹		
FBx_CMD34	DBG0 ²	
FBx_CMD35	DBG1 ²	

Notes:
1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11



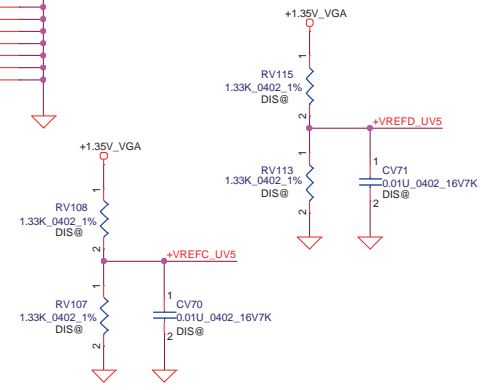
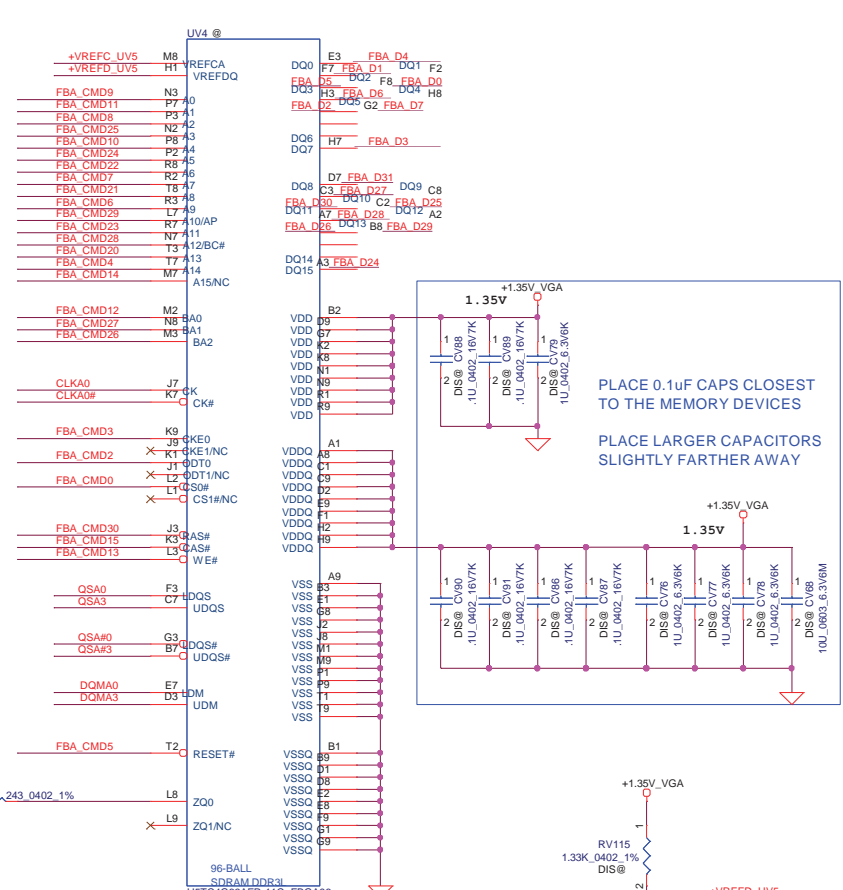
6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPUs support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.

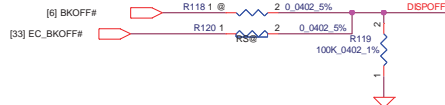
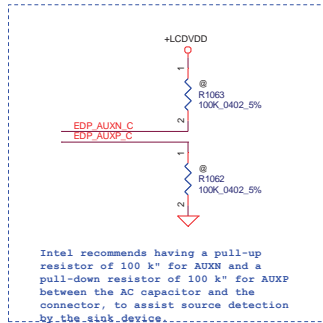
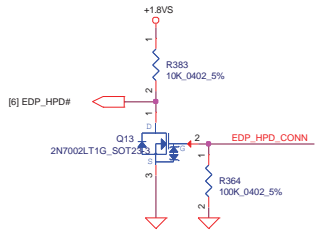
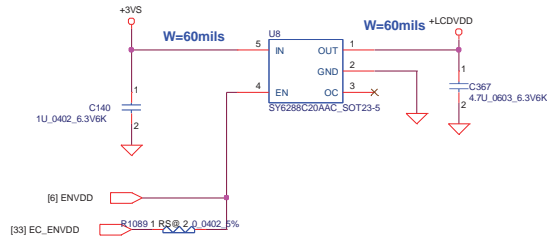
Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for N15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers ¹ . This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

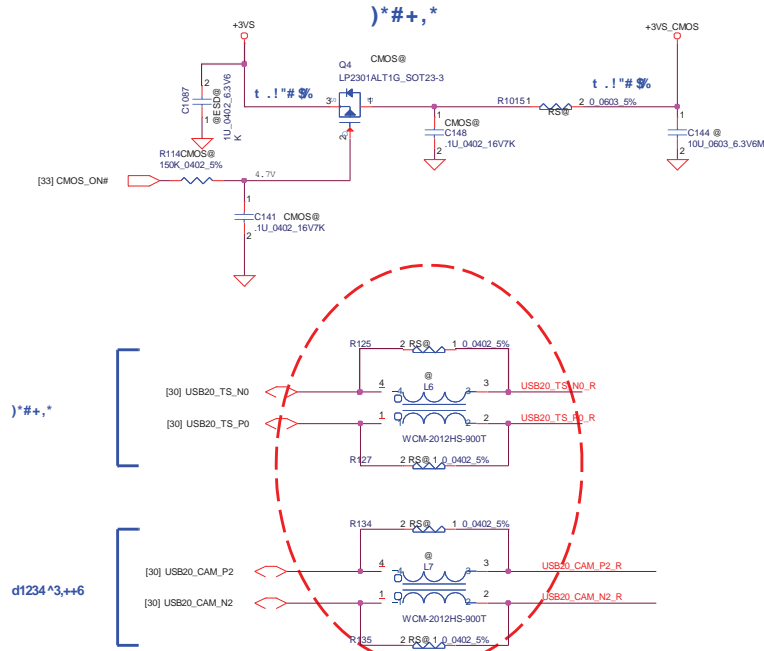
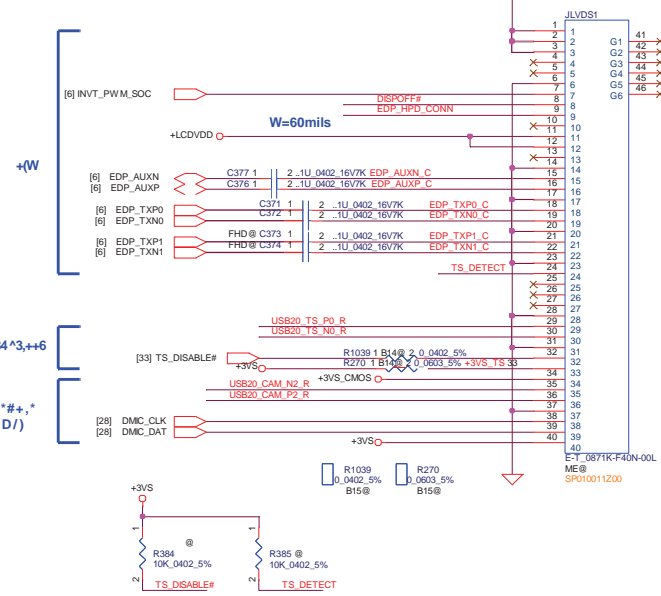
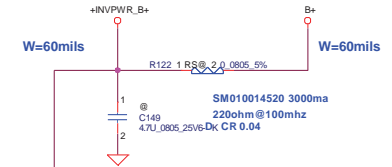
Note: ¹Not including two additional layers for power planes.



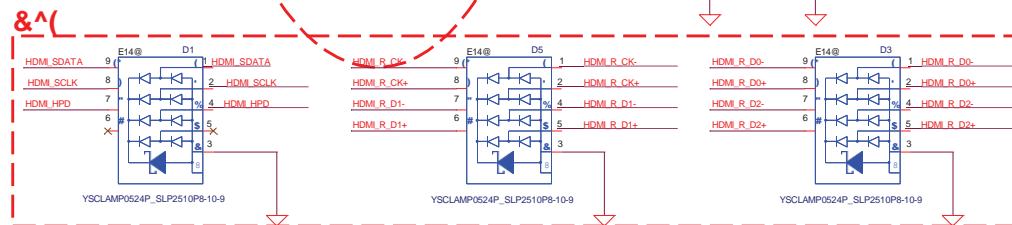
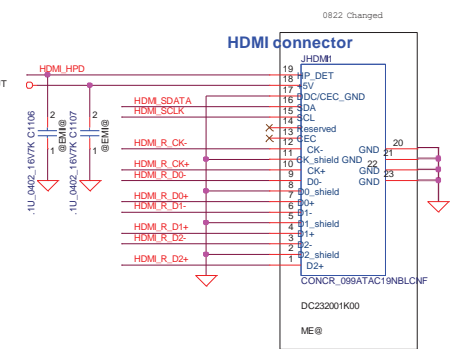
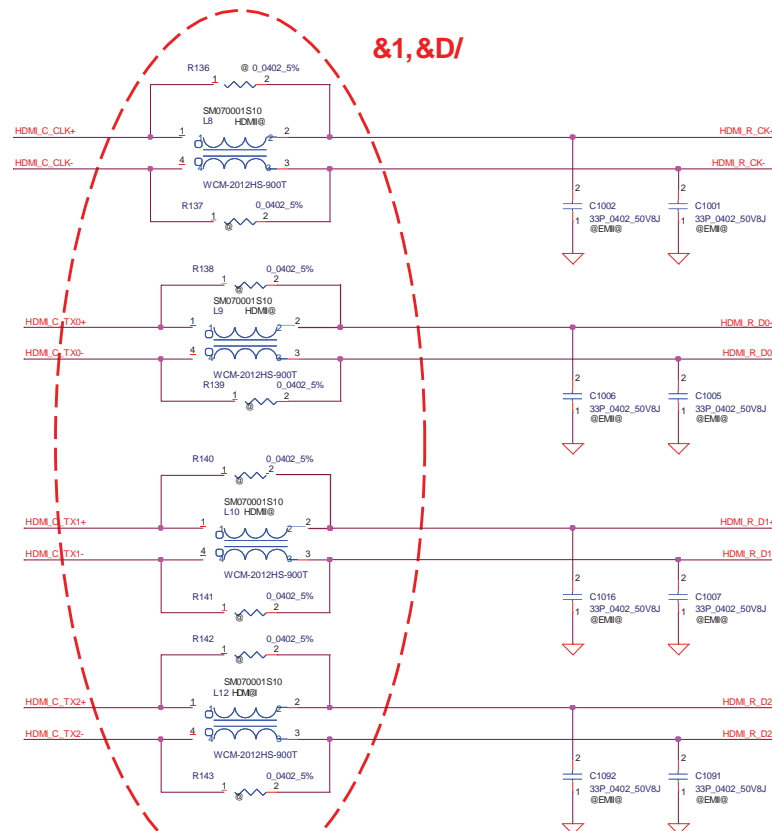
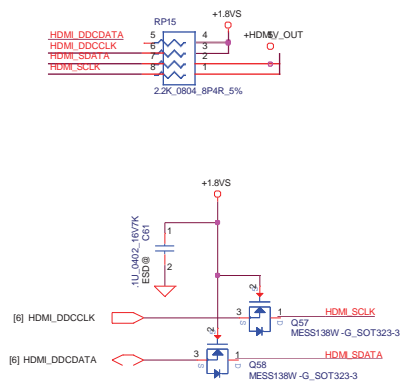
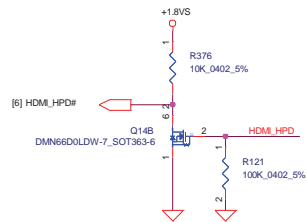
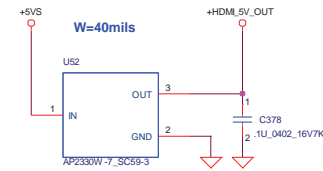
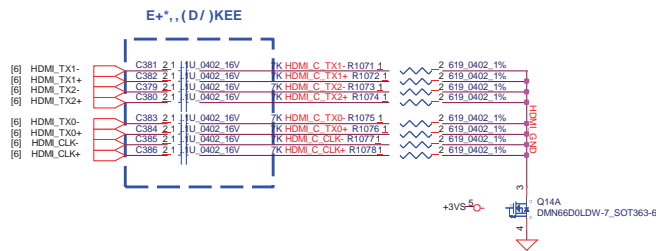
LCD POWER CIRCUIT



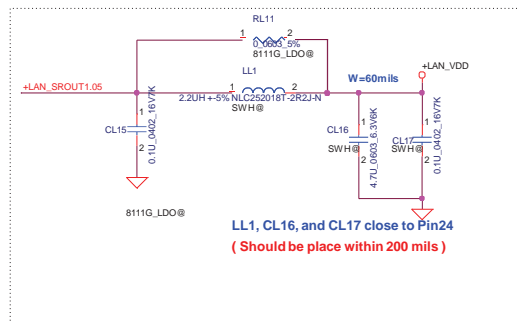
LCD/LED PANEL Conn.



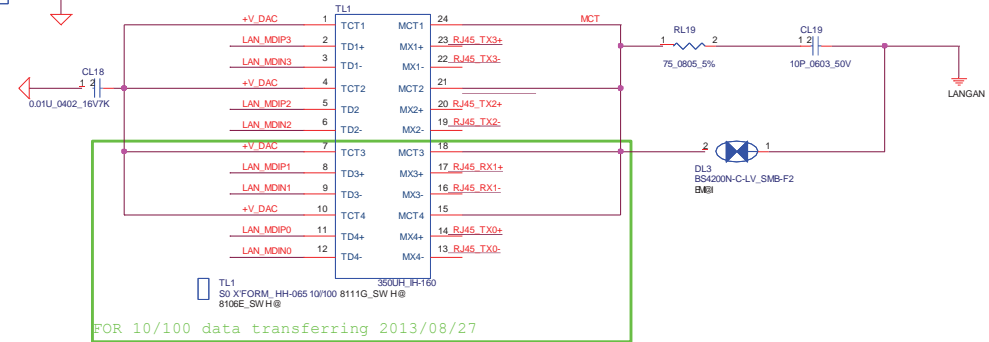
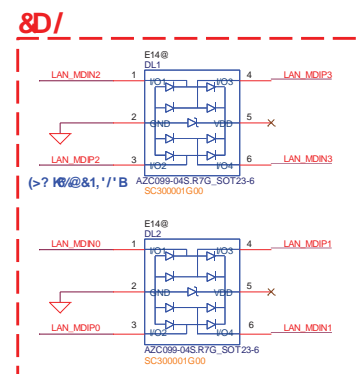
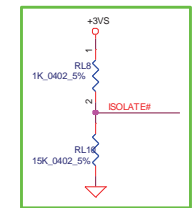
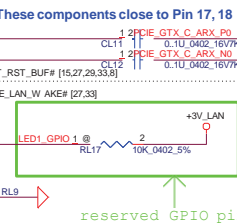
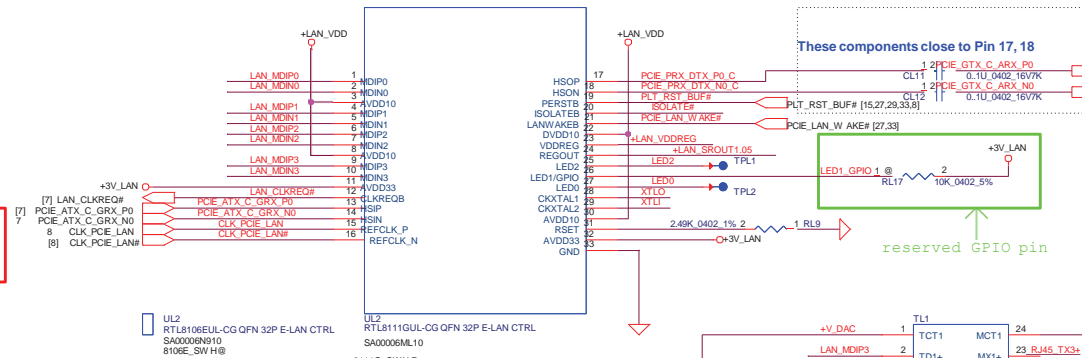
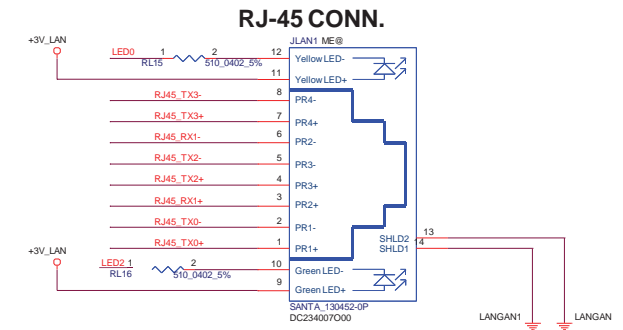
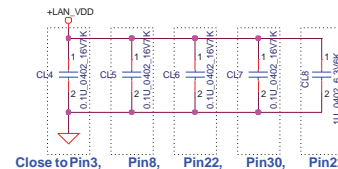
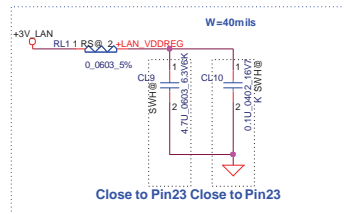
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						Intel BayTrail-M Platform
						Rev 0.1



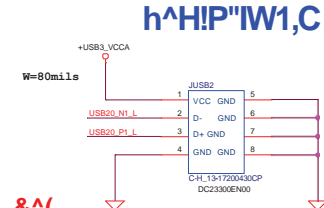
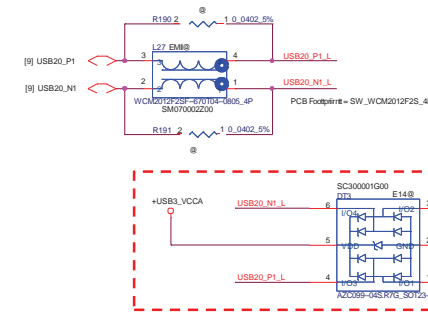
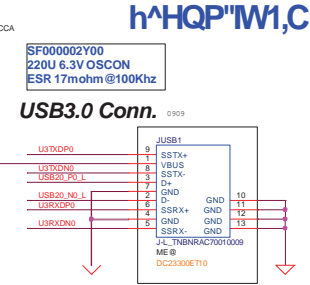
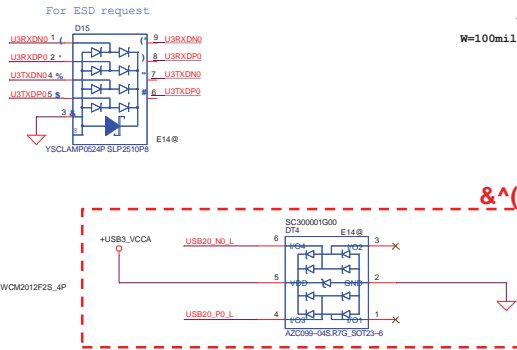
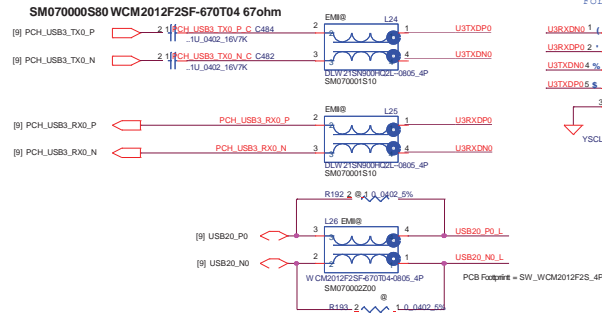
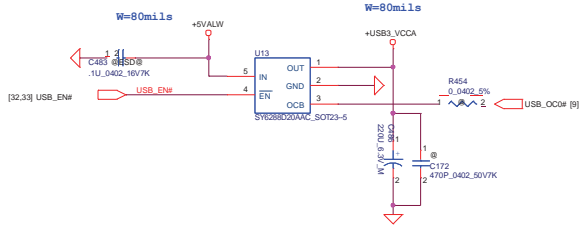
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Custom				Date				Tuesday, February 18, 2014			
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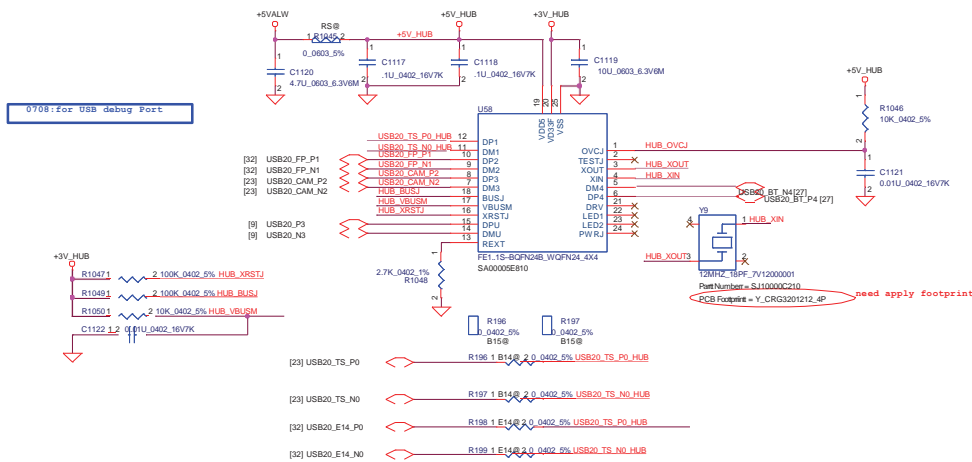
**Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.**



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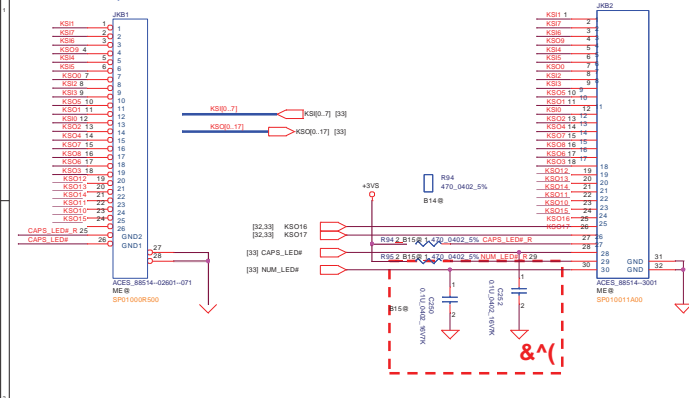


h^H^P", hH



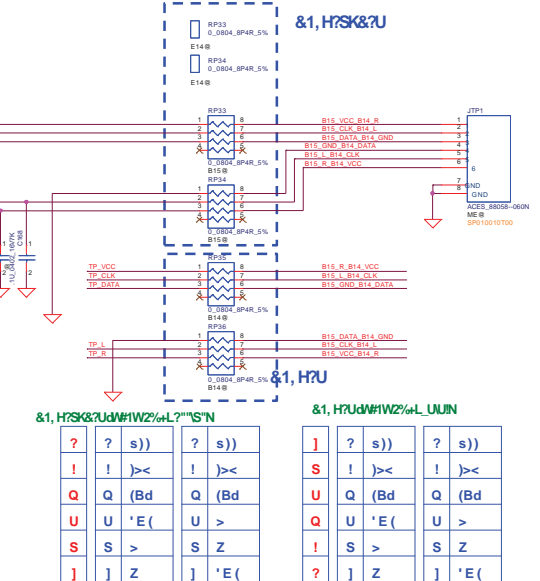
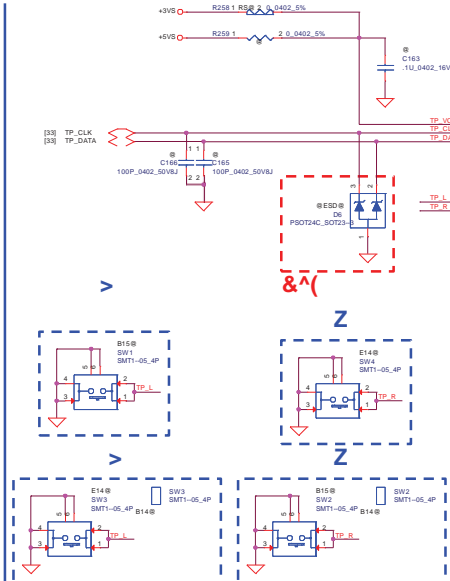
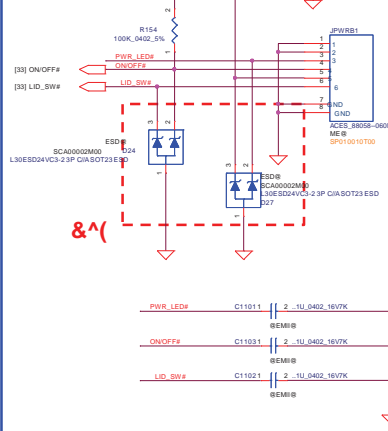
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H&1, HUK&U

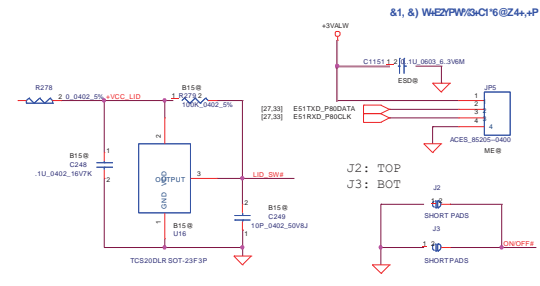
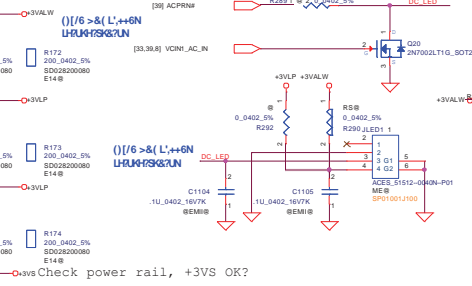
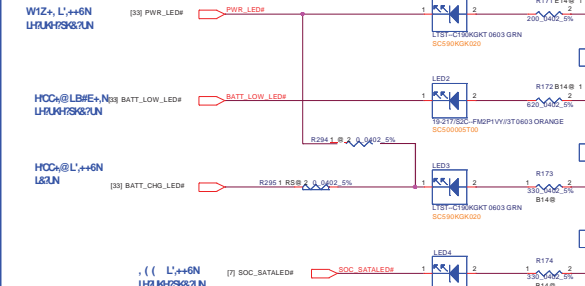
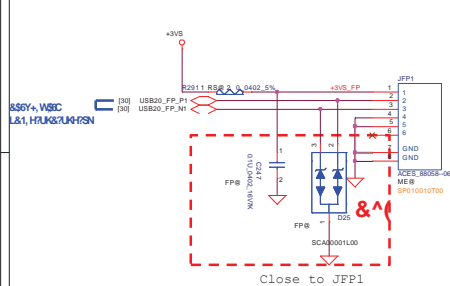


H&1, H7S

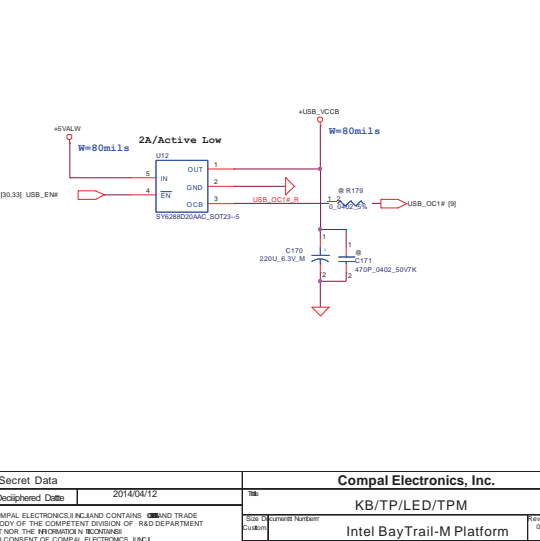
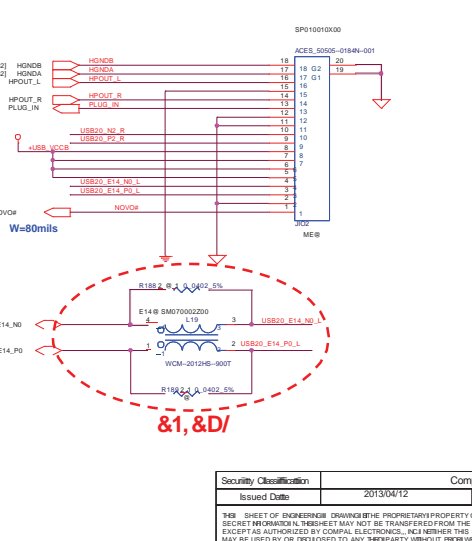
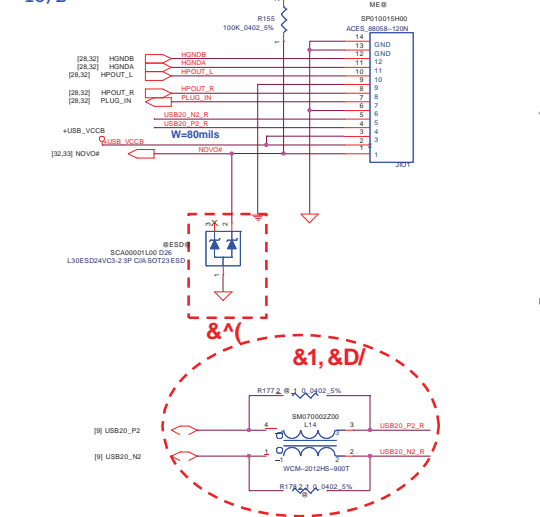
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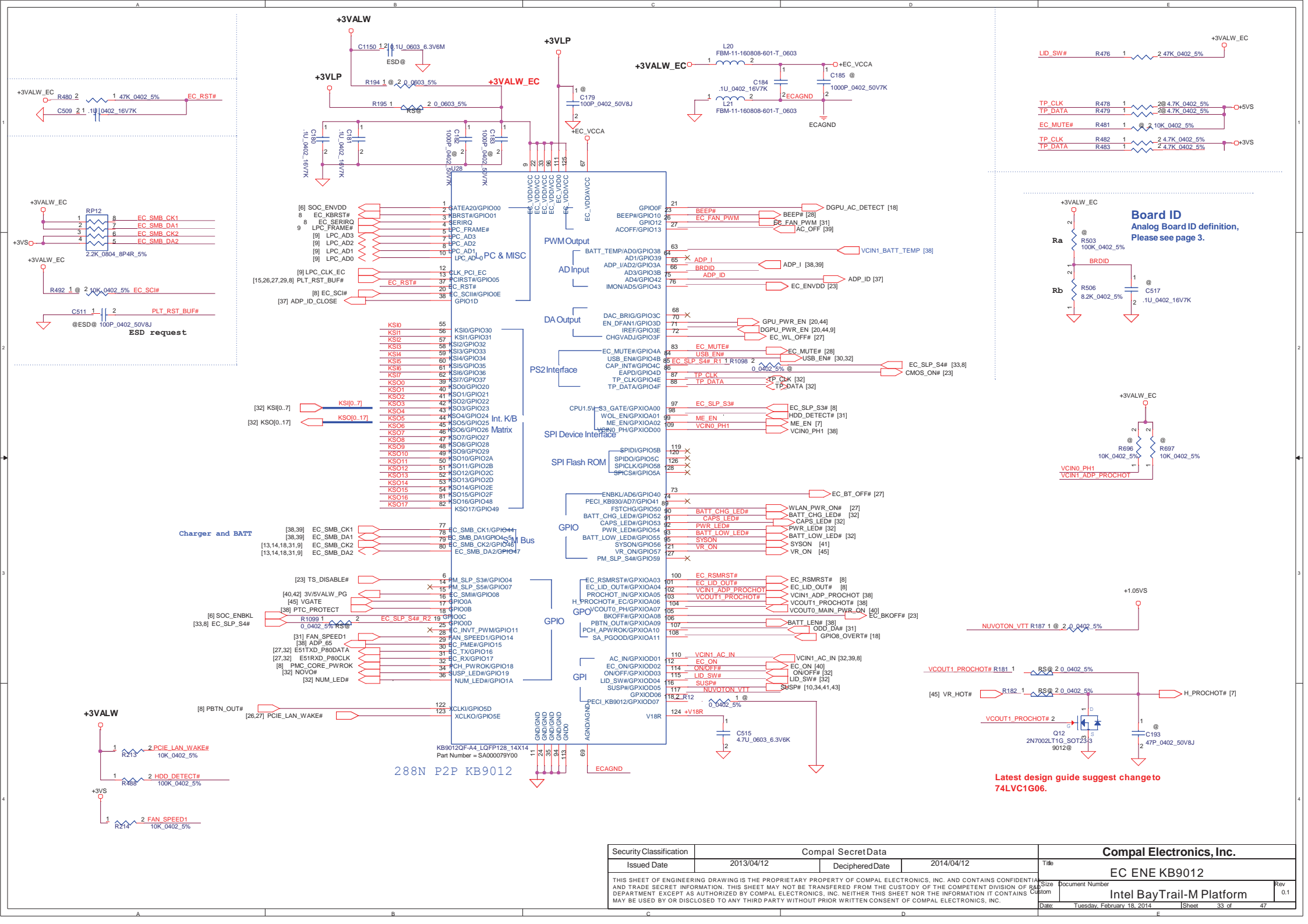


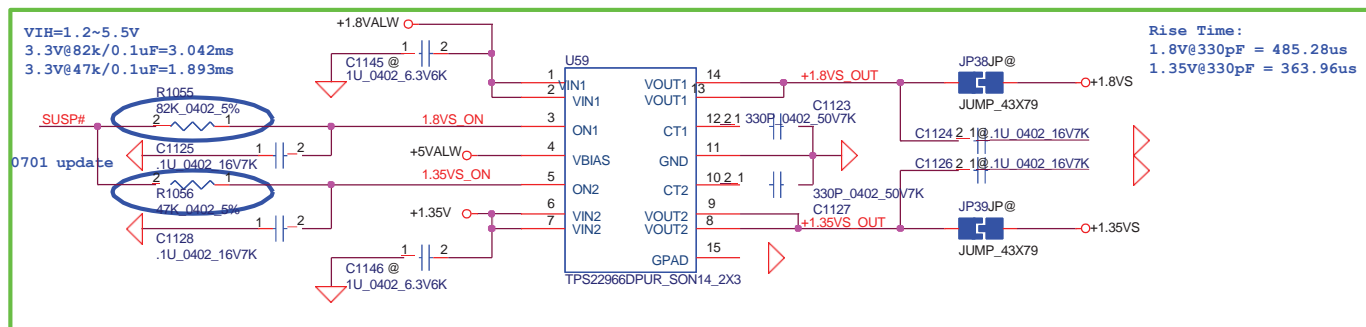
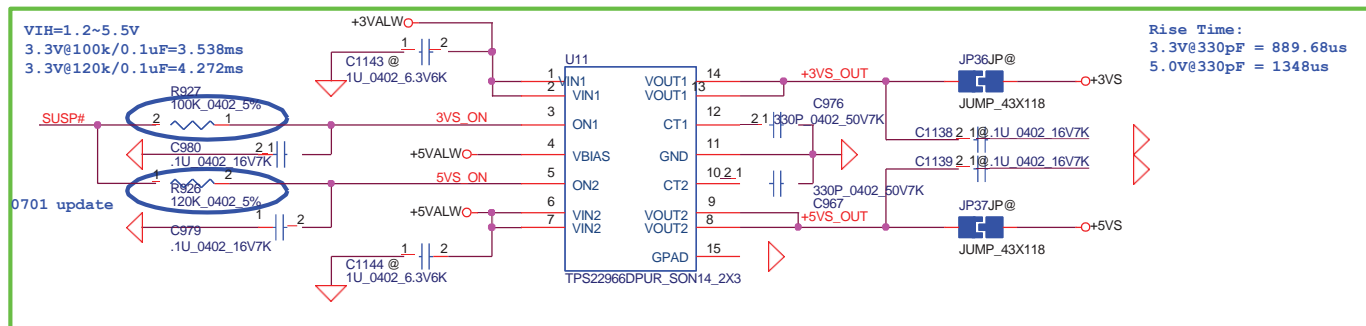
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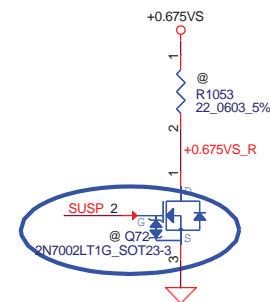
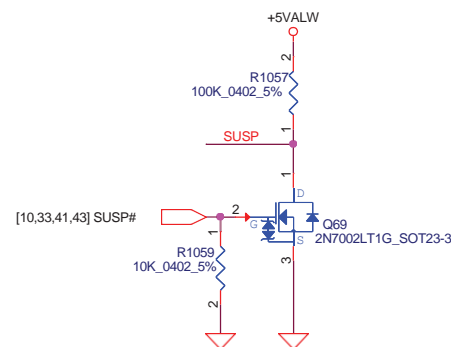
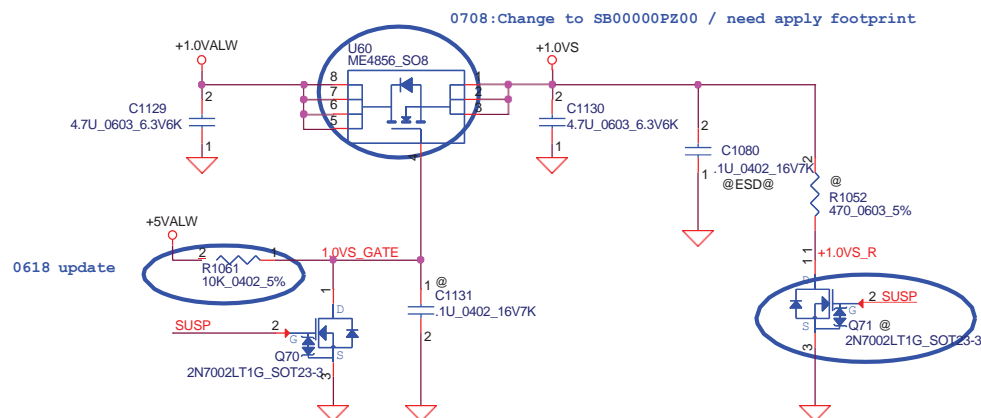
IO/B







+1.0VALW TO +1.0VS



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UG1 GCLK244@

SA000057100

ESD Request

For EMI

SOC_32.768K
NV_VGA
LAN
SOC 25M

Close to GCLK

**Reserved for Swing Level adjustment
(Close GCLK side)**

For EMI

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9-LMRQF0QJH0WVA3B,B5B,LVVC

3DJH" RI" IRU+ : 3,5

WHP	5-DVQIRU RQJH	3*9	ORGLI\ LVW	5-HZUN YHJIA	3DVIH
"	Add Net "EC_SLP_S4#_R1" and "EC_SLP_S4#_R2 by vendor suggestion	33	Add R1098,R1099	V	SIV
!	Reduce component count,delete 12 pcs resister and add 4 pcs row resister.	32	Delete R311,R312,R313,R265,R266,R298,R316,R315, R314,R302,R303,R304, Add RP33,RP34,RP35,RP36	V	SIV
D	Audio vendor suggestion	28	Change CA16,CA13,CA19,CA14 from 0603 to 0402 Change CA11 from 4.7u to 1u , unpop CA17.	V	SIV
F	Nuvoton suggestion to add resister at PIN118 to GND	33	Add R12	V	SIV
G	ESD Team solution		Add C60,C61,C62,C514,C516,C518,C519,C520,D27(reserve)	V	SIV
E	HW strap pin	8	Add R1100,R1101,R1102,R1103,R1104,R1105	V	SIV
H	VGA sequence tuning	20	Add RV23	V	SIV
I	EMI solution	28 & 29	Change RC9 from 0 ohm to 33 ohm POP CA28,CA29,CA30,CA31	V	SIV
J	ESD solution		Add C1080,C1081,C1082,C1083,C1084,C1085,C1086,C1087,C1088	V	SIV
"K	EMI solution for DDR DIMM	10	Reserve C1189,C1190,L51,L52	V	SIV
"	ESD request to delete XDP test point	8	Delete T198,T199,T200,T209,T210,T211,T212	V	SIV
!"	EMI request	10	Change R1017 from shortPAD to 0 ohm	V	SIV
"D	Delete 0 ohm due to 15'' ODD can short direct	31	Delete R130,R131,R132,R133	V	SIV
"F	ME request	31	Modify H35 footprint to H_6P0,H8 & H9 to H_3P3		SIT
"G	ME request	31	Change JODD2 P/N from SP01001RS00 to SP011312061		SIT
"E	Protect EC	23	JLVDS1 pin 6 pull down	V	SIT
"H	Vendor request	33	Modify U11.111 connect to +3VLP only,C179.1 connect to +3VLP	V	SIT
"I	Vendor suggestion	20	+1.05VS to +1.05VS_VGA power switch enable pin reserve DGPU_PWR_EN path	V	SIT
"J	Sourcer suggestion	31	Change Q2407,Q2408 P/N from SB000008E00 to SB000002R00	V	SIT
!K	EMI request		Reserve C1001,C1002,C1005,C1006,C1007,C1016,C1091,C1092,C1101, C1102,C1103,C1104,C1105,C1106,C1107	V	SIT
!"	ESD request		Add C1149,C1150,C1151,C1152,C1153,C1154	V	SIT

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